STUDY AND ANALYSIS OF THREE PHASE MULTILEVEL INVERTER

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF

Bachelor of Technology

in

Electrical Engineering

By

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CERTIFICATE

This is to certify that the thesis entitled, "STUDY AND ANALYSIS OF THREE PHASE MULTILEVEL INVERTER" submitted by Sri **Sanjeev Balachandran, Sunil Hansdah, A. Narendra Babu** in partial fulfillments for the requirements for the award of Bachelor of Technology Degree in Electrical Engineering at National Institute of Technology, Rourkela (Deemed University) is an authentic work carried out by him under my supervision and guidance.

To the best of our knowledge, the matter embodied in the thesis has not been submitted to any other University / Institute for the award of any Degree or Diploma.

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ACKNOWLEDGEMENT

I wish to express my deep sense of gratitude and indebtedness to Prof. A.K.Panda, Department of Electrical Engineering, N.I.T Rourkela for introducing the present topic and for his inspiring guidance, constructive criticism and valuable suggestion throughout this project work.

I would like to express my gratitude to Dr. P. K. Nanda (Head of the Department), for his valuable suggestions and encouragements at various stages of the work. I am also thankful to all staff members of Department of Electrical Engineering NIT Rourkela.

May 2007

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CONTENT

ABSTRACT

The present project deals with study and analysis of three phase multilevel inverters and their different topologies and configurations. The main purpose of our study is to study the modulation techniques and compare them with each other analyzing their advantages and disadvantages. Their applications have been analyzed according to their functioning such as the cascaded inverter for example could also serve as a rectifier/charger for the batteries of an electric vehicle while the vehicle was connected to an ac supply.

In our thesis, the three main multi-level inverters studied are cascading H bridge, diode clamped and flying capacitor structure. The term multilevel converter is utilized to refer to a power electronic circuit that could operate in an inverter or rectifier mode.

One first impression of a multilevel power converter is that the large number of switches may lead to complex pulse-width modulation (PWM) switching algorithms. However, early developments in this area demonstrated the relatively straightforward nature of multilevel PWM. Our project presents the fundamental methods as well as reviews some novel research. The methods are divided into the traditional voltage-source and current-regulated methods. Some discrete current-regulated methods are presented herein, but due to their nature, the harmonic performance is not as good as that of voltage-source methods. Voltage-source methods also more easily lend themselves to digital signal processor (DSP) or programmable logic device (PLD) implementation.

Although we have discussed numerous topologies and modulation methods, several more can be found. An additional goal of this project is to introduce concepts related to reducing the number of isolated voltage sources and sensors. This can be important in the high power quality cascaded multilevel inverters which require several voltage sources and knowledge of the dc voltage levels.

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Chapter 1

GENERAL INTRODUCTION

Background

Objective

1.1 Introduction

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application.

The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three-level converter . Subsequently, several multilevel converter topologies have been developed . However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

1.2 Advantages and Disadvantages

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows.

- **Staircase waveform quality:** Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.

- **Common-mode (CM) voltage:** Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies

- **Input current:** Multilevel converters can draw input current with low distortion.

- **Switching frequency:** Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

Unfortunately, multilevel converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex.

Plentiful multilevel converter topologies have been proposed during the last two decades Contemporary research has engaged novel converter topologies and unique modulation schemes. Moreover, three different major multilevel converter structures have been reported in the literature: cascaded H-bridges converter with separate dc sources, diode clamped (neutral-clamped), and flying capacitors (capacitor clamped). Moreover, abundant modulation techniques and control paradigms have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others. In addition, many multilevel converter applications focus on industrial medium-voltage motor drives , utility interface for renewable energy systems, flexible AC transmission system (FACTS), and traction drive systems.

Chapter 2

MULTI-LEVEL INVERTER STRUCTURES

Cascaded H Bridge Inverters

Diode Clamped Inverters

Flying Capacitor Inverters

Other Structures

2.1 Cascaded H-Bridges

A single-phase structure of an m-level cascaded inverter is illustrated in Figure.2.1. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1, S_2, S_3, and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 2.1. The phase voltage v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}. For a stepped waveform such as the one depicted in Figure 2.2 with s steps, the Fourier Transform for this waveform follows :

$$H(n) = \frac{4}{\pi n}\left[\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s)\right], \quad \text{where } n = 1, 3, 5, 7, \ldots$$

... 2.1
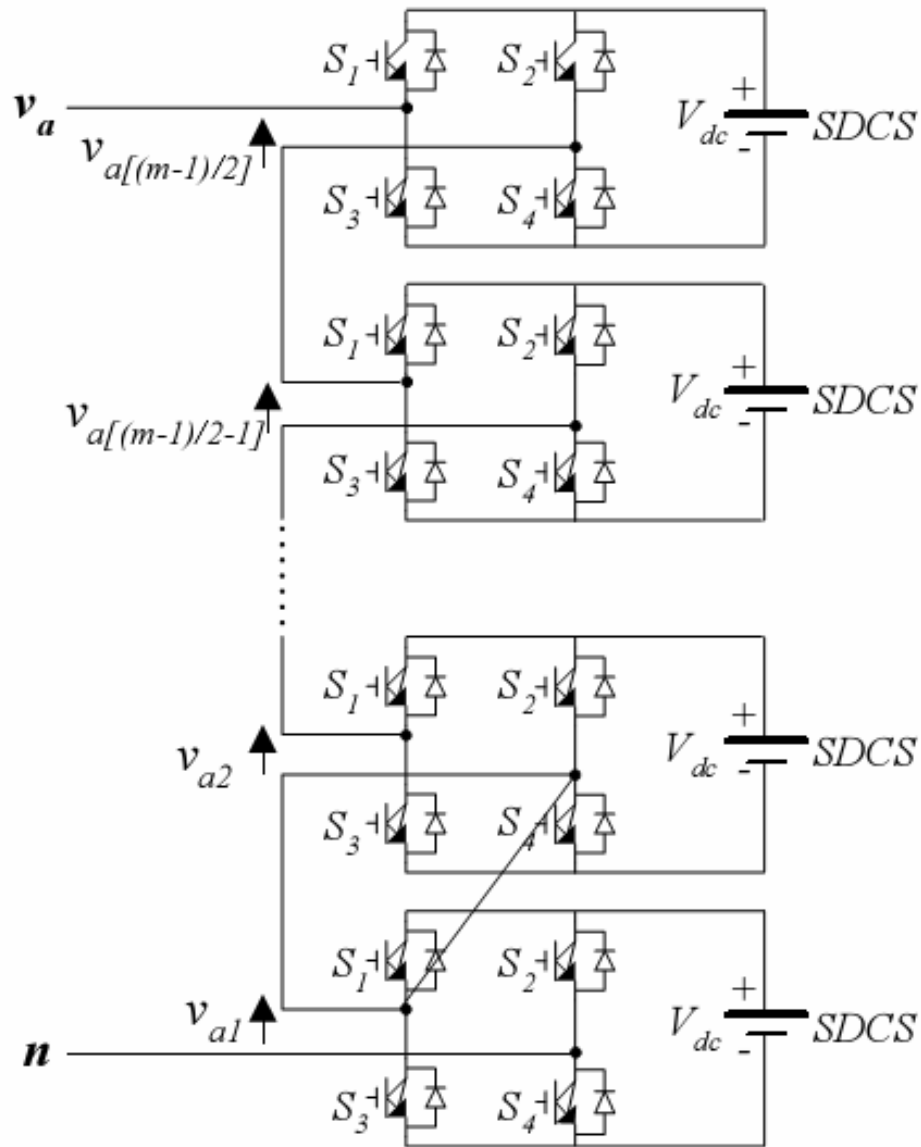
Fig 2.1. Single-phase structure of a multilevel cascaded H-bridges inverter.
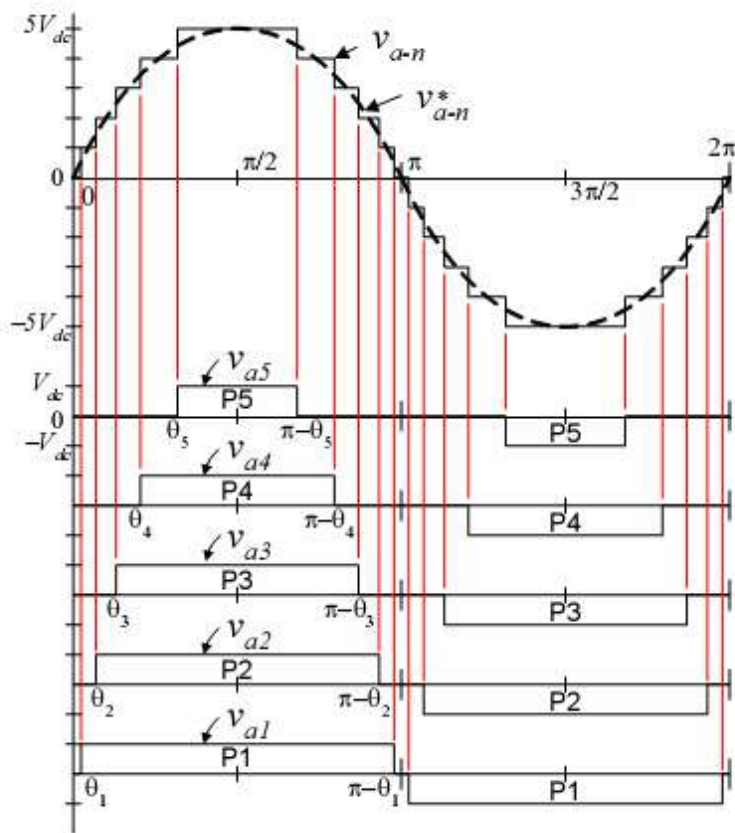
Fig.2.2 Output phase voltage waveform of an 11-level cascade inverter with 5 separate dc sources.

The conducting angles 1.2.3..s can be chosen such that the voltage total harmonic distortion is a minimum. Generally, these angles are chosen so that predominant lower frequency harmonics, 5th, 7th, 11th, and 13th , harmonics are eliminated. More detail on harmonic elimination techniques will be presented in the next section. Multilevel cascaded inverters have been proposed for such applications as static var generation, an interface with renewable energy sources, and for battery-based applications. Three-phase cascaded inverters can be connected in wye, as shown in Figure 3, or in delta. Peng has demonstrated a prototype multilevel cascaded static var generator connected in parallel with the electrical system that could supply or draw reactive current from an electrical system . The inverter could be controlled to either regulate the power factor of the current drawn from the source or the bus voltage of the electrical system where the inverter was connected. Peng and Joos have also shown that a cascade inverter can be directly connected in series with the electrical system for static var compensation. Cascaded inverters are ideal for connecting renewable energy sources

with an ac grid, because of the need for separate dc sources, which is the case in applications such as photovoltaics or fuel cells. Cascaded inverters have also been proposed for use as the main traction drive in electric vehicles, where several batteries or ultracapacitors are well suited to serve as SDCSs .

The cascaded inverter could also serve as a rectifier/charger for the batteries of an electric vehicle while the vehicle was connected to an ac supply as shown in Figure 2.3. Additionally, the cascade inverter can act as a rectifier in a vehicle that uses regenerative braking.
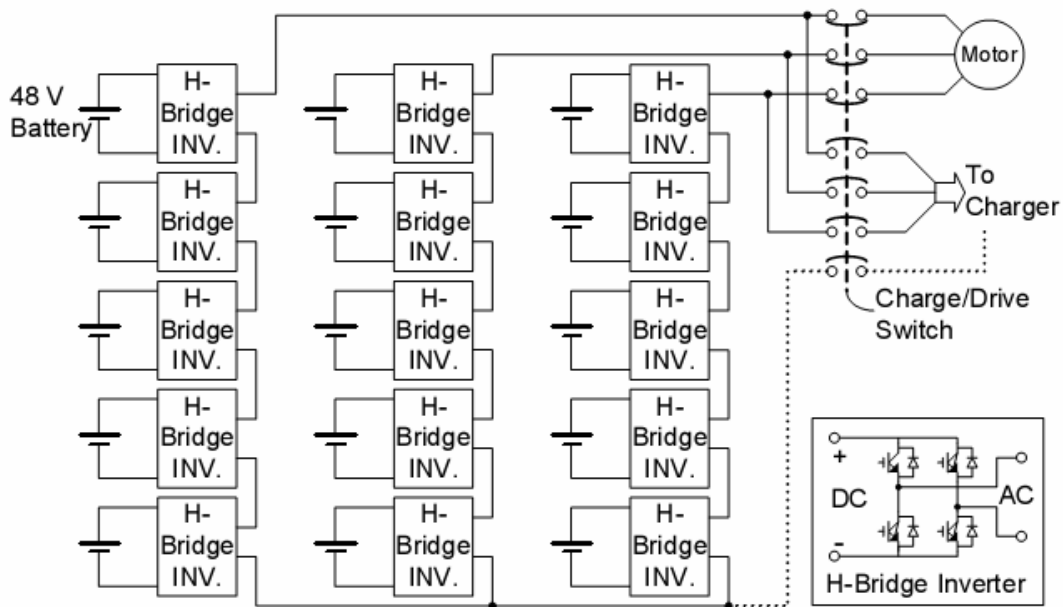
Fig 2.3. Three-phase wye-connection structure for electric vehicle motor drive and battery charging.

Manjrekar has proposed a cascade topology that uses multiple dc levels, which instead of being identical in value are multiples of each other. He also uses a combination of fundamental frequency switching for some of the levels and PWM switching for part of the levels to achieve the output voltage waveform. This approach enables a wider diversity of output voltage magnitudes; however, it also results in unequal voltage and current ratings for each of the levels and loses the advantage of being able to use identical, modular units for each level. The main advantages and disadvantages of multilevel cascaded H-bridge converters are as follows :

Advantages:

- The number of possible output voltage levels is more than twice the number of dc sources (m = 2s + 1).

- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

Disadvantages:

- Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple SDCSs readily available.

Another kind of cascaded multilevel converter with transformers using standard three-phase bi-level converters has been proposed. The circuit is shown in Figure 2.4. The converter uses output transformers to add different voltages. In order for the converter output voltages to be added up, the outputs of the three converters need to be synchronized with a separation of 120^0 between each phase. For example, obtaining a three-level voltage between outputs a and b, the output voltage can be synthesized by $V_{ab} = V_{a1-b1} + V_{b1-a2} + V_{a2-b2}$. An isolated transformer is used to provide voltage boost. With three converters synchronized, the voltages V_{a1-b1}, V_{b1-a2}, V_{a2-b2}, are all in phase; thus, the output level can be tripled .

The advantage of the cascaded multilevel converters with transformers using standard three-phase bi-level converters is the three converters are identical and thus control is more simple. However, the three converters need separate DC sources, and a transformer is needed to add up the output voltages.
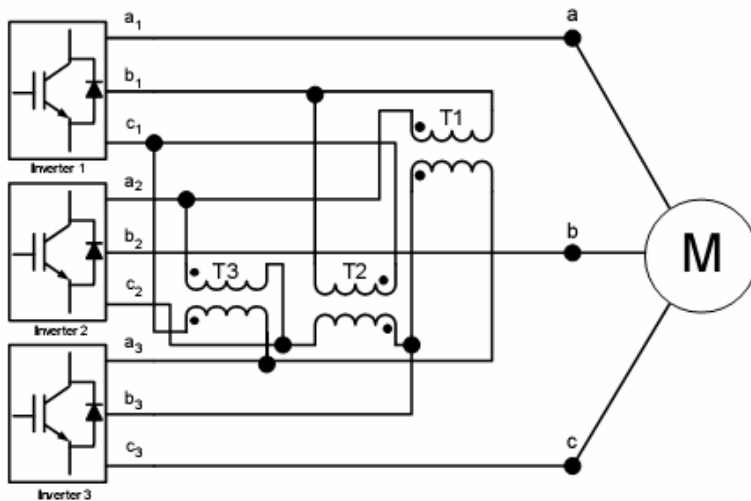

Fig.2.4. Cascaded multilevel converter with transformers using standard three-phase bi-level converters.

2.2. Diode-clamped multilevel inverter

The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series bank of capacitors. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was introduced. However, with an even number of voltage levels, the neutral point is not accessible, and the term multiple point clamped (MPC) is sometimes applied. Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been mostly limited to the three-level. Because of industrial developments over the past several years, the three-level inverter is now used extensively in industry applications. Although most applications are medium-voltage, a three-level inverter for 480V is on the market.

Figure 2.5. shows the topology of the three-level diode-clamped inverter. Although the structure is more complicated than the two-level inverter, the operation is straightforward and well known. In summary, each phase node (a, b, or c) can be connected to any node in the capacitor bank (d_0 ,d_1 ,d_2).Connection of the a-phase to junctions d_0 and d_2 can be accomplished by switching transistors T_{a1} andT_{a2} both off or both on respectively. These states are the same as the two-level inverter yielding a line-to-ground voltage of zero or the dc voltage. Connection to the junction d_1 is accomplished by gating T_{a1} off and T_{a2} on. In this representation, the labels T_{a1} and T_{a2} are used to identify the transistors as well as the transistor logic (1=on and 0=off). Since the transistors are always switched in pairs, the complement transistors are labeled Ta1 and T_{a2} accordingly. In a practical implementation, some dead time is inserted between the transistor signals and their complements meaning that both transistors in a complementary pair may be switched off for a small amount of time during a transition . However, for the discussion herein, the dead time will be ignored. From Figure2.5, it can be seen that, with this switching state, the a-phase current i_{as} will flow into the junction through diode as D_{a1} if it is negative or out of the junction through diode D_{a2} if the current is are positive. According to this description, the inverter relationships for the presented in Table 2.1.

Table 2.1. Three level Inverter Relationships

s_a	T_{a2}	T_{a1}	v_{ag}	i_{adc1}	i_{adc2}
0	0	0	0	0	0
1	0	1	v_{c1}	i_{as}	0
2	1	1	$v_{c1} + v_{c2}$	0	i_{as}

If each capacitor is charged to one-half of the dc voltage, then the line-to-ground and voltage can be calculated. The dc currents i_{adc1} and i_{adc2} are the a-phase components to the junction currents in Figure2.5 respectively.

The general n-level modulator, described in the next section, determines the switching state for each phase. For practical implementation, the switching state needs to be converted into transistor signals. Considering Table .2-1, this can be accomplished in general by

$$T_{ai} = \begin{cases} 1 & s_a \geq i \\ 0 & \text{elesewise} \end{cases}$$

... 2.2

An inverse relationship may also be useful and is given by

$$s_a = \sum_{i=1}^{n-1} T_{ai}$$

...2.3

Once the transistor signals are established, general expressions for the a-phase line-to-ground voltage and the a-phase component of the dc currents can be written as

$$v_{ag} = \sum_{i=1}^{n-1} T_{ai} v_{ci}$$

...2.4

$$i_{adci} = [T_{a(i+1)} - T_{ai}] i_{as} \quad \text{for } i = 1, 2, \ldots (n-2)$$

...2.5
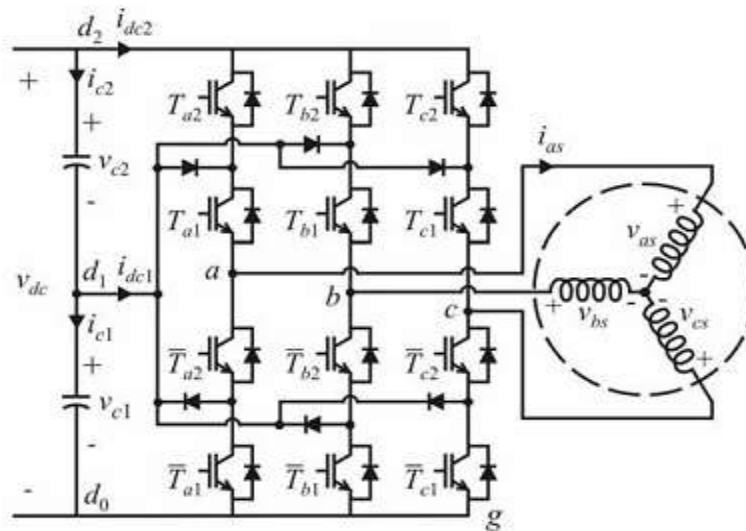
Figure 2.5.   3 level Diode clamped inverter topology

2.3 Flying capacitor structure

Another fundamental multilevel topology, the flying capacitor, involves series connection of capacitor clamped switching cells. This topology has several unique and attractive features when compared to the diode-clamped inverter. One feature is that added clamping diodes are not needed. Furthermore, the flying capacitor inverter has switching redundancy within the phase which can be used to balance the flying capacitors so that only one dc source is needed.

Figure .2.6 shows the three-level flying capacitor inverter. The general concept of operation is that each flying capacitor is charged to one-half of the dc voltage and can be connected in series with the phase to add or subtract this voltage. Table 2.2 shows the relationships for the a-phase:

Table 2.2 Three level flying capacitors relationships

s_a	T_{a2}	T_{a1}	v_{ag}	i_{ac1}	i_{adc}
0	0	0	0	0	0
1	0	1	v_{ac1}	$-i_{as}$	0
	1	0	$v_{dc} - v_{ac1}$	i_{as}	i_{as}
2	1	1	v_{dc}	0	i_{as}

In comparison to the three-level diode-clamped inverter, an extra switching state is possible. In particular, there are two transistor states which make up the level $s_a = 1$ Considering the direction of the a-phase flying capacitor current i_{ac1} for the redundant states, a decision can be made to charge or discharge the capacitor and therefore, the capacitor voltage can be regulated to its desired value by switching within the phase. In Table 2.2, the current i_{adc} is the a-phase component of the dc current. The total dc current can be calculated by summing the components for all phases.

As with the three-level flying capacitor inverter, the highest and lowest switching states do not change the charge of the capacitors. The two intermediate voltage levels contain enough redundant states that both capacitors can be regulated to their ideal voltages.

For the general n-level flying capacitor inverter, the transistor voltages can be determined from the transistor signals by

$$v_{Tai} = (1-T_{ai})\left[v_{aci} - v_{ac(i-1)} - I_a v_{sw} + (1-I_a)v_d\right] \\ + T_{ai}\left[I_a v_{sw} - (1-I_a)v_d\right]$$

...2.7

When employing eqn 2.7, the lowest and highest capacitor voltages will be $v_{ac0} = 0$.
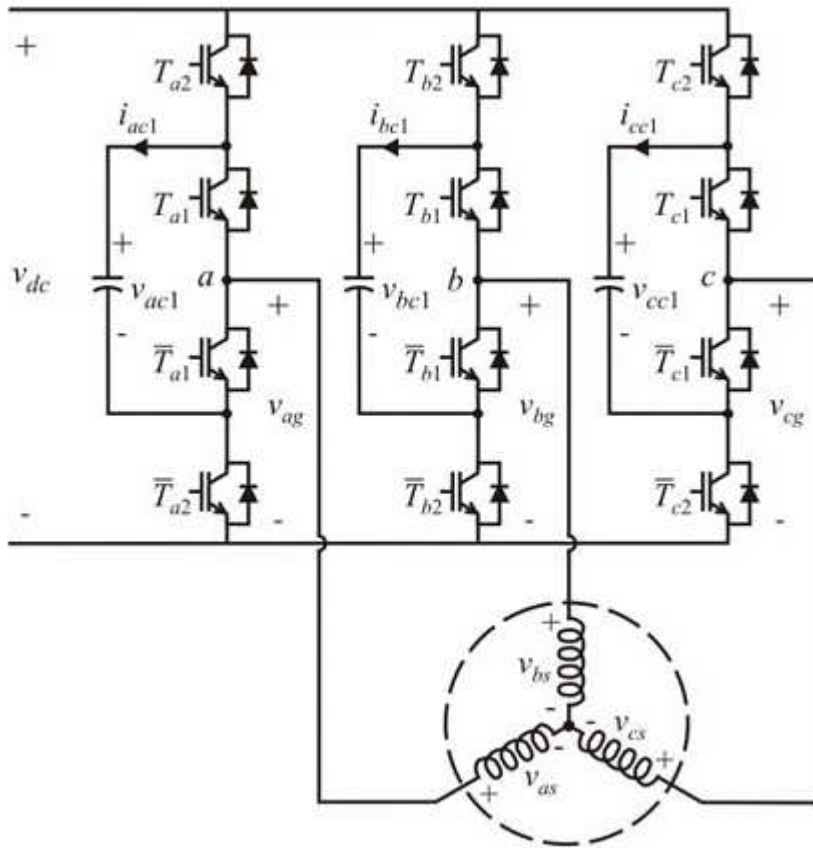
Figure 2.6 Three level flying capacitor topology

2.4 Other Multilevel Inverter Structures

Besides the three basic multilevel inverter topologies previously discussed, other multilevel converter topologies have been proposed; however, most of these are "hybrid" circuits that are combinations of two of the basic multilevel topologies or slight variations to them. Additionally, the combination of multilevel power converters can be designed to match with a specific application based on the basic topologies.   In the interest of completeness, some of these will be identified and briefly described.

A. Generalized Multilevel Topology

Existing multilevel converters such as diode-clamped and capacitor-clamped multilevel converters can be derived from the generalized converter topology called P2 topology proposed by Peng as illustrated in Figure 2.7. The generalized multilevel converter topology can balance each voltage level by itself regardless of load characteristics, active or reactive power conversion and without any assistance from other circuits at any number of levels automatically. Thus, the topology provides a complete multilevel topology that embraces the existing multilevel converters in principle.

Figure 2.7 shows the P2 multilevel converter structure per phase leg. Each switching device, diode, or capacitor's voltage is 1 V , for instance, 1/ (m-1) of the DC-link voltage. Any dc converter with any number of levels, including the conventional bi-level converter can be obtained using this generalized topology.
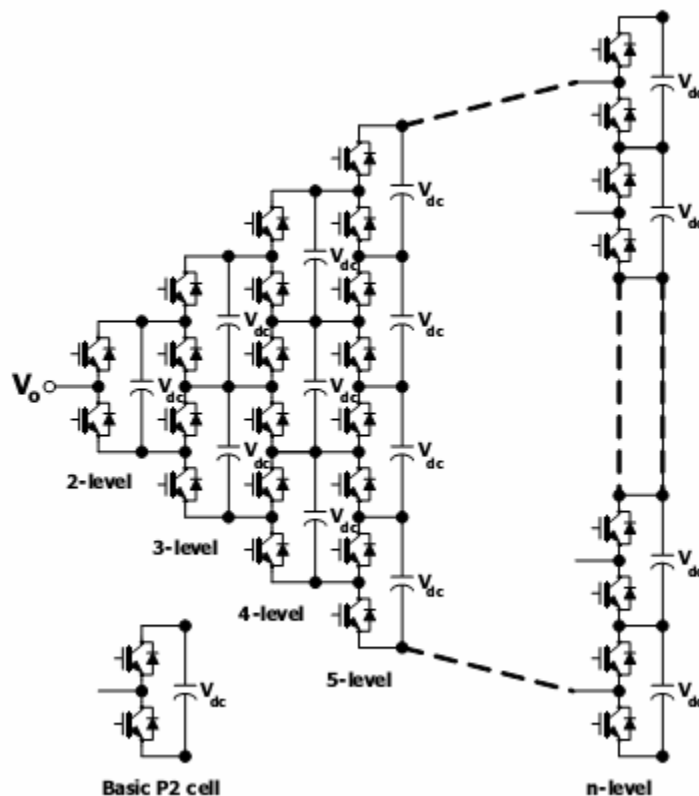

Fig 2.7 Generalized P2 multilevel converter topology for one phase leg.

B. Mixed-Level Hybrid Multilevel Converter

To reduce the number of separate DC sources for high-voltage, high-power applications with multilevel converters, diode-clamped or capacitor-clamped converters could be used to replace the full-bridge cell in a cascaded converter. An example is shown in Figure 2.8. The nine-level cascade converter incorporates a three-level diode-clamped converter as the cell. The original cascaded H-bridge multilevel converter requires four separate DC sources for one phase leg and twelve for a three-phase converter. If a five-level converter replaces the full-bridge cell, the voltage level is effectively doubled for each cell. Thus, to achieve the same nine voltage levels for each phase, only two separate DC sources are needed for one phase leg and six for a three-phase converter. The configuration has mixed-level hybrid multilevel units because it embeds multilevel cells as the building block of the cascade converter. The advantage of the topology is it needs less separate DC sources. The disadvantage for the topology is its control will be complicated due to its hybrid structure.
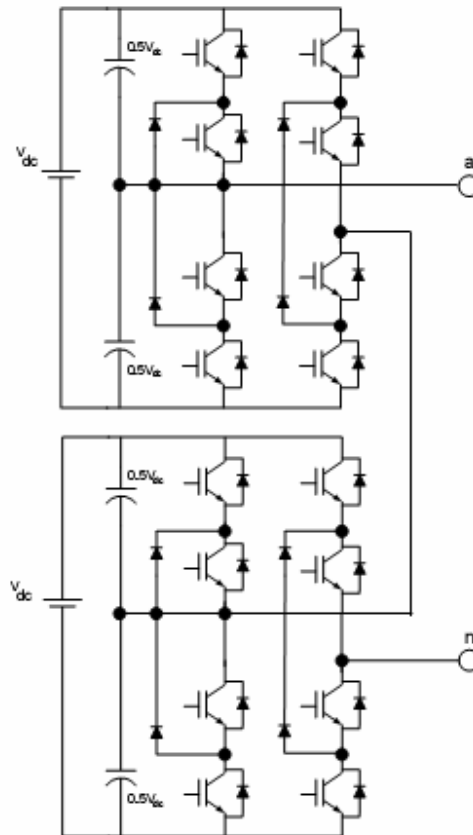
Fig 2.8 Mixed-level hybrid unit configuration using the three-level diode-clamped

converter as the cascaded converter cell to increase the voltage levels.

C. Soft-Switched Multilevel Converter

Some soft-switching methods can be implemented for different multilevel converters to reduce the switching loss and to increase efficiency. For the cascaded converter, because each converter cell is a bi-level circuit, the implementation of soft switching is not at all different from that of conventional bi-level converters. For capacitor-clamped or diode-clamped converters, soft-switching circuits have been proposed with different circuit combinations. One of soft-switching circuits is a zero-voltage-switching type which includes auxiliary resonant commutated pole (ARCP), coupled inductor with zero-voltage transition (ZVT), and their combinations as shown in Figure 2.9.
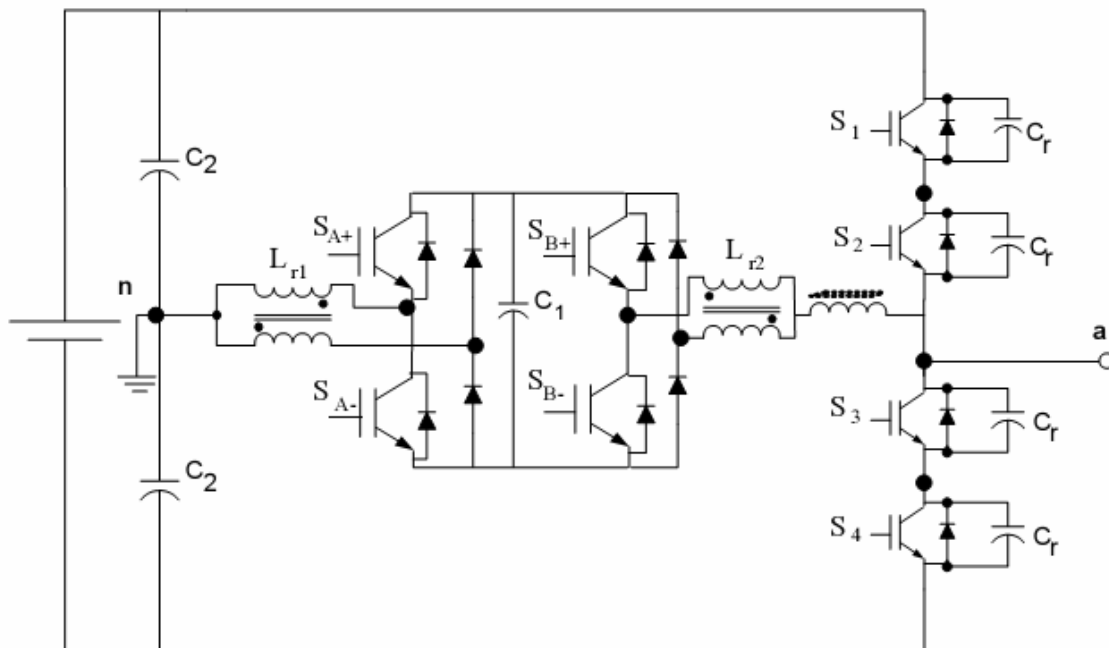
Fig 2.9 Zero-voltage switching capacitor-clamped inverter circuit.

D. Back-to-Back Diode-Clamped Converter

Two multilevel converters can be connected in a back-to-back arrangement and then the combination can be connected to the electrical system in a series-parallel arrangement as shown in Figure 2.10. Both the current demanded from the utility and the voltage delivered to the load can be controlled at the same time. This series-parallel active power filter has been referred to as

a universal power conditioner when used on electrical distribution systems and as a universal power flow controller when applied at the transmission level. The diode-clamped inverter has been chosen over the other two basic multilevel circuit topologies for use in a universal power conditioner for the following reasons:

- All six phases (three on each inverter) can share a common dc link. Conversely, the cascade inverter requires that each dc level be separate, and this is not conducive to a back-to-back arrangement.

- The multilevel flying-capacitor converter also shares a common dc link; however, each phase leg requires several additional auxiliary capacitors. These extra capacitors would add substantially to the cost and the size of the conditioner.

Because a diode-clamped converter acting as a universal power conditioner will be expected to compensate for harmonics and/or operate in low amplitude modulation index regions, a more sophisticated, higher-frequency switch control than the fundamental frequency switching method will be needed.
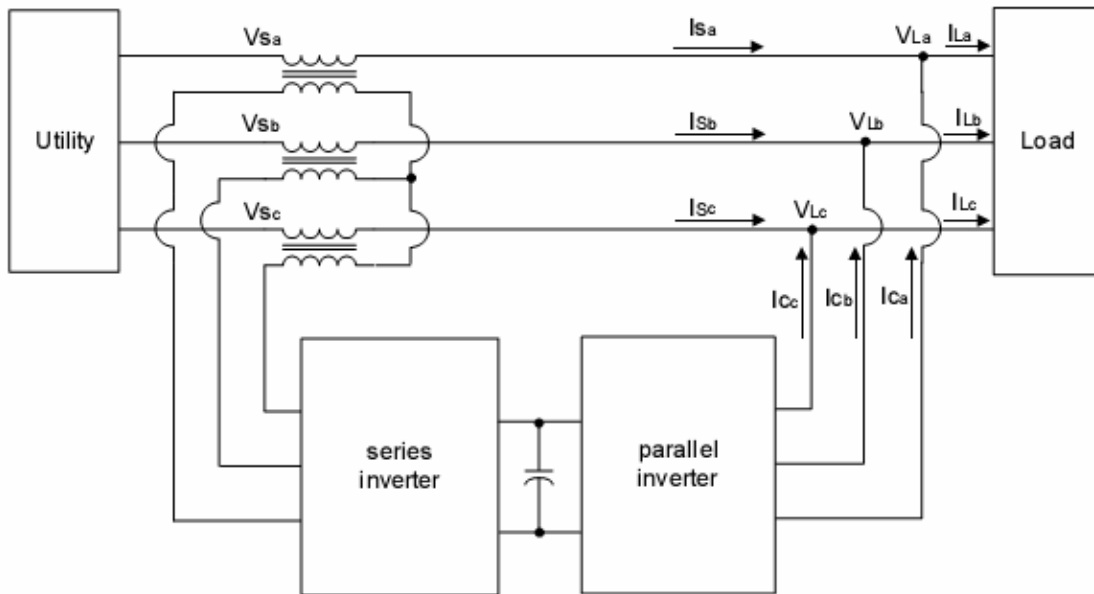

Fig. 2.10 Series-parallel connection to electrical system of two back-to-back inverters.

Chapter 3

MODULATION TECHNIQUES

Voltage Control Methods
Current Control Methods

3. Multilevel Modulation

This chapter presents the fundamental methods pulse-width modulation (PWM) .The methods are divided into the traditional voltage-source and current-regulated methods. An advantage of the current-regulated methods is that there is a need to control the current directly since the higher-level control (vector control, reactive power control, active rectifier, etc.) nearly always outputs commanded currents. However, current controls typically depend on event scheduling and are therefore analog implementations which can only be reliably operated up to a certain power level. Some discrete current-regulated methods are presented herein, but due to their nature, the harmonic performance is not as good as that of voltage-source methods. Voltage-source methods also more easily lend themselves to digital signal processor (DSP) or programmable logic device (PLD) implementation.

3.1 Voltage-source methods

Voltage-source modulation has taken two major paths; sine triangle modulation in the time domain and space vector modulation in the q-d stationary reference frame. Sine-triangle and space vector modulation are exactly equivalent in every way. Adjusting some parameters in the sine-triangle scheme (such as the triangle shape and sine wave harmonics) is equivalent to adjusting other parameters in the space vector scheme (such as the switching sequence and dwell time). A general tradeoff between harmonics and switching losses has been identified for multilevel inverters.

The inverter line-to-ground voltage can be directly controlled through the switching state. For a specific inverter, the switching state is broken out into transistor signals. However, as a control objective, it is more desirable to regulate the line-to-neutral voltages of the load. Infinite set of line-to-ground voltages for a desired set of line-to-neutral voltages since the matrix has a zero determinate. This provides some flexibility in the line-to ground voltages since any common-mode terms included will not appear on the load. In a three-phase system, the common terms include dc offset and any triplen harmonics. To narrow the possibilities, the commanded line-to-ground voltages will be defined herein as:

$$\begin{bmatrix} v_{ag}^* \\ v_{bg}^* \\ v_{cg}^* \end{bmatrix} = \frac{m\,v_{dc}}{2} \begin{bmatrix} \cos(\theta_c) \\ \cos\left(\theta_c - \frac{2\pi}{3}\right) \\ \cos\left(\theta_c + \frac{2\pi}{3}\right) \end{bmatrix} + \frac{v_{dc}}{2} \left[1 - \frac{m}{6}\cos(3\theta_c) \right] \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$$

$$...3.1$$

where m is the modulation index which has a range of

$$0 \le m \le \frac{2}{\sqrt{3}}$$

$$...3.2$$

and θ_c is the converter electrical angle. In eqn 3.1, first set of terms on the right hand side define a sinusoidal set of commanded voltages with controllable amplitude and frequency through m and θ_c respectively. The second set of terms on the right hand side is the common-mode terms. In this case, a dc offset is applied so that the commanded line-to-ground voltages will be within the allowable range of zero to the dc voltage. The other common-mode term is a third harmonic component which is added to fully utilize the dc source voltage. The common-mode terms of are just the minimum set and it is possible to command other types of line-to-ground voltages, including discontinuous waveforms, in order to optimize switching frequency or harmonics.

Some fundamental definitions will now be presented for reference when describing the modulation methods. First, duty cycles are defined by scaling the commanded voltages with modifications to account for multiple voltage levels. The modified duty cycles are

$$\begin{bmatrix} d_{am} \\ d_{bm} \\ d_{cm} \end{bmatrix} = \left(\frac{n-1}{2} \right) \begin{bmatrix} m\cos(\theta_c) \\ m\cos\left(\theta_c - \frac{2\pi}{3}\right) \\ m\cos\left(\theta_c + \frac{2\pi}{3}\right) \end{bmatrix} + \left(\frac{n-1}{2} \right) \left[1 - \frac{m}{6}\cos(3\theta_c) \right] \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$$

$$... 3.3$$

Next, a commanded voltage vector is defined by

$$v_{qds}^{s*} = v_{qs}^{s*} - j\,v_{ds}^{s*}$$

$$...3.4$$

where the commanded q- and d-axis voltages are related to the a-b-c variables of 3.1

$$v_{qs}^{s*} = \frac{2}{3}v_{ag}^{*} - \frac{1}{3}v_{bg}^{*} - \frac{1}{3}v_{cg}^{*}$$

...3.5

$$v_{ds}^{s*} = \frac{1}{\sqrt{3}}\left(v_{cg}^{*} - v_{bg}^{*}\right)$$

...3.6

It should be pointed out that the commanded q- and d-axis voltages can also be defined in terms of desired line-to-neutral voltages since the zero sequence is being ignored.

A. Sine-triangle modulation

One of the most straightforward methods of describing voltage-source modulation is to illustrate the intersection of a modulating signal (duty cycle) with triangle waveforms. Figure 3.1 demonstrates the sine-triangle method for a nine-level inverter.

Therein, the a-phase duty cycle is compared with eight (n-1 in general) triangle waveforms. The switching rules are simply

$$s_{ai} = \begin{cases} 1 & d_{am} > tri \\ 0 & \text{elsewise} \end{cases}$$

$$s_a = \sum_{i=1}^{n-1} s_{ai}$$

...3.7
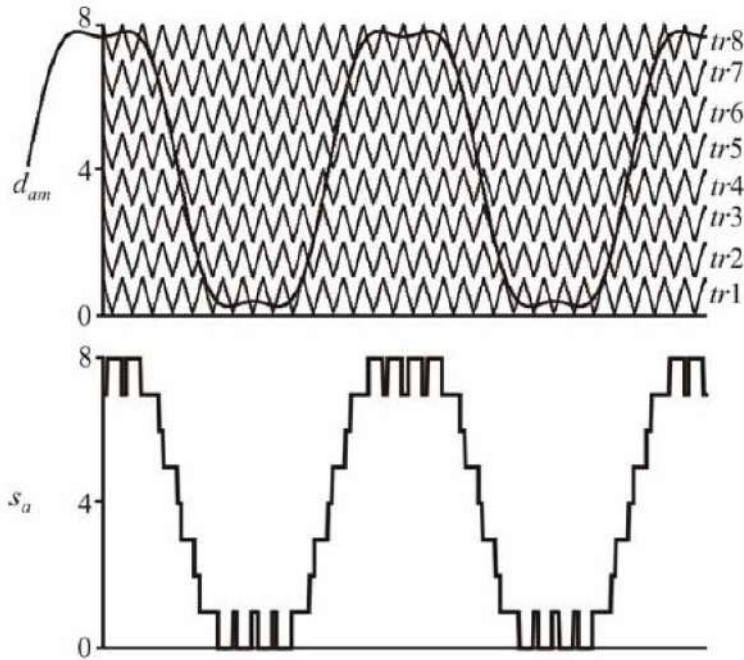
Fig 3.1 Nine Level Sine Triangle Modulation

B. Space vector modulation

Space vector modulation (SVM) is based on vector selection in the q-d stationary reference frame. As an example, consider the commanded voltage vector defined by 3.4. For a four-level system, the commanded vector is plotted along with the vectors obtainable by the inverter in Figure 3.2. The desired vector v_{qds}^{s*} is shown at some point in time, but will follow the circular path if a three-phase set of voltages are required on the load. Although the circular path shown in the figure, the path may be arbitrary. The first step in the SVM scheme is to identify the three nearest vectors. In this example, they are v_{52} , v_{56} , and the redundant vectors v_{36} and v_{57}. The next step is to determine the amount of time that must be spent at each vector in order for the average voltage to be equal to the commanded voltage. This can be done using some simple mathematical relationships. In particular, the vectors and their corresponding times are related by:

$$v_{36,57}T_{36,57} + v_{52}T_{52} + v_{56}T_{56} = v_{qds}^{s*}T_{sw}$$

…3.8

where T_{sw} is the switching time of the PWM control which is the total of the time spent at each vector or

$$T_{sw} = T_{36,57} + T_{52} + T_{56}$$

…3.9

Based on 3.8 and 3.9 the amount of time for each voltage vector can be computed by solving the inverse problem

$$\begin{bmatrix} \mathrm{Re}\{v_{36,57}\} & \mathrm{Re}\{v_{52}\} & \mathrm{Re}\{v_{56}\} \\ \mathrm{Im}\{v_{36,57}\} & \mathrm{Im}\{v_{52}\} & \mathrm{Im}\{v_{56}\} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} T_{36,57} \\ T_{52} \\ T_{56} \end{bmatrix} = \begin{bmatrix} \mathrm{Re}\{v_{qds}^{s*}\} \\ \mathrm{Im}\{v_{qds}^{s*}\} \\ T_{sw} \end{bmatrix}$$

…3.10

The final step in the SVM scheme is to determine a sequence of switching for the voltage vectors. For this example, the switching sequence could be from v_{57} to v_{56} to v_{52} to v_{36} .At the end of the sequence, the controller switching time T_{sw} has elapsed and the process is repeated with updating the commanded voltage, identifying the three nearest vectors, calculating the switching times, and scheduling the switching sequence.

As can be seen, there are a lot of free parameters in this process. The time spent at vectors v_{56} and v_{52} (sometimes called dwell time) is directly determined by 3.10, but the time spent at vectors v_{57} and v_{36} is an arbitrary split of $T_{36,57}$. Whether this time is split evenly or as a function of the commanded voltage angle can have an effect on the inverter harmonics and switching losses. Instead of splitting the time, the sequence could be changed to switch from v_{57} to v_{56} to v_{52} which would reduce commutation. the sequence can also be reversed by switching from v_{52} to v_{56} to v_{57} which will affect the harmonics.

C. Discrete implementation

One attractive feature of voltage-source PWM methods is that they can be readily implemented on a DSP/PLD control. Figure 3.3 demonstrates a per-phase time domain method of implementing PWM in a discrete time system for a four-level inverter. Therein, the modified

a-phase duty cycle is shown along with the switching state output of the modulator. At each point in time, the *a*-phase duty cycle is updated based on the magnitude and phase of the commanded voltages in accordance with 3.3. The continuous calculation is shown in Figure 3.2 and is a small portion of the duty cycle shown in Figure 3.1. In a DSP system, discrete values of the duty cycle are computed which are represented by points in Figure 3.3. This creates a zero-order-hold effect which is negligible if the switching frequency is large compared to the changes in the duty cycle. In order to schedule the switching state transitions during the switching period, the nearest lower and upper voltage levels are determined. This is a simple matter of intergerizing the duty cycle using

$$ll_a = \text{INT}(d_{am})$$

...3.11

$$ul_a = ll_a + 1$$

...3.12

where INT is the intergerization function that returns the nearest integer less than or equal to its argument. Next, a switching time for each *a*-phase is determined based on the proximity to the lower level by direct calculations. For the *a*-phase, this is calculated by

$$t_a = (d_{am} - ll_a)T_{sw}$$

...3.13

As can be seen, the switching time t_a will range from zero to 100% of the switching period and is the time that should be spent at the upper level. The final step is scheduling the switching transitions. In Figure 3.3, the pulse is left-justified in the switching period starting at the upper level and transitioning to the lower level. The scheduling rules for this type of justification are

$$s_a = \begin{cases} ul_a & 0 \le t' \le t_a \\ ll_a & t_a < t' \le T_{sw} \end{cases}$$

...3.14

where t ' is time that is zero at the beginning of the switching period. The same procedure is applied to the *b*- and *c*-phases.

Usually, the nearest levels and switching times for each phase are calculated in a DSP. This information is then transferred to a PLD which operates at a higher a higher clock frequency and can make the transitions of the switching state on a nanosecond time scale. In a practical

implementation, the DSP and PLD clocks are tied together by a PLD circuit which divides its clock and sends a clock signal to the DSP on the microsecond time scale. Besides the zero-order hold effect, there is a one-sample delay effect which is caused by the fact that the DSP will take some time to determine the levels and switching times. This effect is not shown in Figure 3.3, but the computed duty cycle (indicated by the discrete points) is used in the following switching period causing a lag between the duty cycle and the switching state. This effect is negligible for high switching frequencies.

Some comments are appropriate to show the equivalence between the discrete implementation and the sine-triangle and SVM methods. The example shown in Figure 3.3 assumed that the switching state would start in the upper level and transition to the lower level at the appropriate time. An identical switching pattern is obtained in the sine-triangle method by using a saw-tooth waveform instead of a triangle waveform as shown in Figure 3.1. Likewise, moving the pulses to the right side of the switching period (a transition from the lower level to the upper level) would be equivalent to using a reverse saw-tooth waveform. If the pulses are centered within the switching period, then the result is the same as that using a triangle waveform. Since the sine-triangle and discrete methods are both performed on a per-phase basis and in the time domain, their equivalence is easily understood. The equivalence to SVM can be seen by creating a plot of the switching states for all three phases as shown in Figure 3.4. Therein the switching for a four level inverter is shown over one switching period. In this example, the c-phase switches from level 1 to 0 with the shortest switching time (lowest duty cycle). The b-phase switches from 2 to 1 with an intermediate time representing a duty cycle greater than the c-phase. The a-phase switches from level 3 to 2 with the highest duty cycle. The result of switching the three phases is that four windows are created by the switching boundaries. The first window (where $s_a = 3$, $s_b = 2$, and $s_c = 1$) creates vector v_{57} according to 3.1 to 3.7. The next three windows create vectors v_{56}, v_{52}, and v_{36}. These are the same three nearest vectors in the example used in the section on SVM. The sequence is also the same. However, the sequence can be reversed in the discrete implementation by switching to right justification. In a similar way, the sequence can be reversed in the SVM method. There is much more to the equivalence of these methods including adding harmonics to the duty cycles in the sine-triangle method or changing the dwell times in the SVM method.

It can be seen that the discrete method presented herein relies on computation directly from the duty cycles and therefore it is not necessary to define triangle waveforms or

voltage vectors. However, sine-triangle modulation is useful in that it can provide a straightforward method of describing multilevel modulation. Also, the SVM method leads to an insightful (and sometimes simpler) way to view the operation of multilevel inverters.
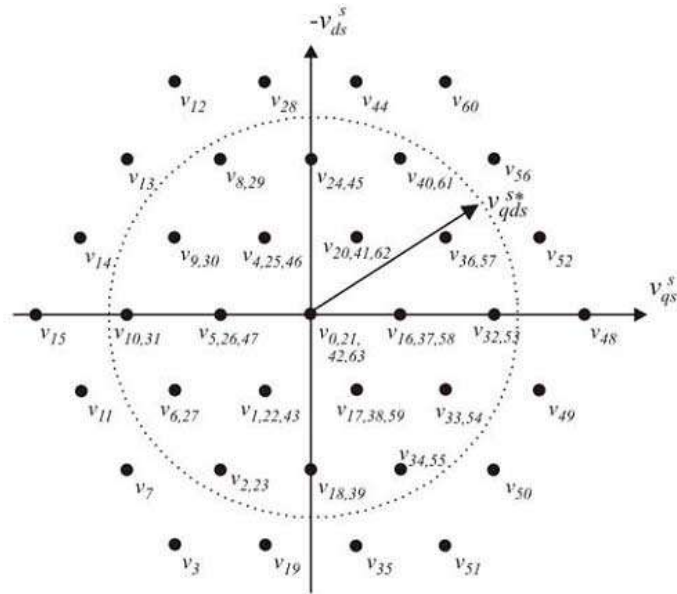

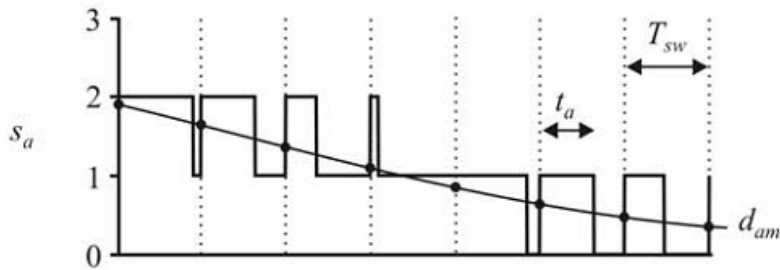**Fig 3.2 Four level inverter space vector modulation.**

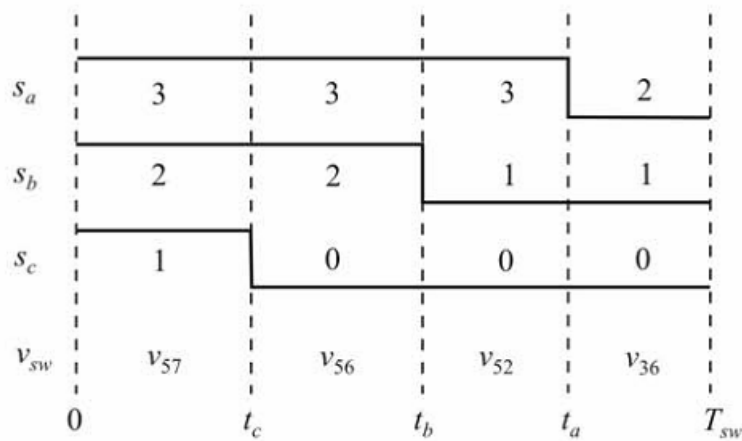**Fig 3.3. Per phase discrete modulation.**

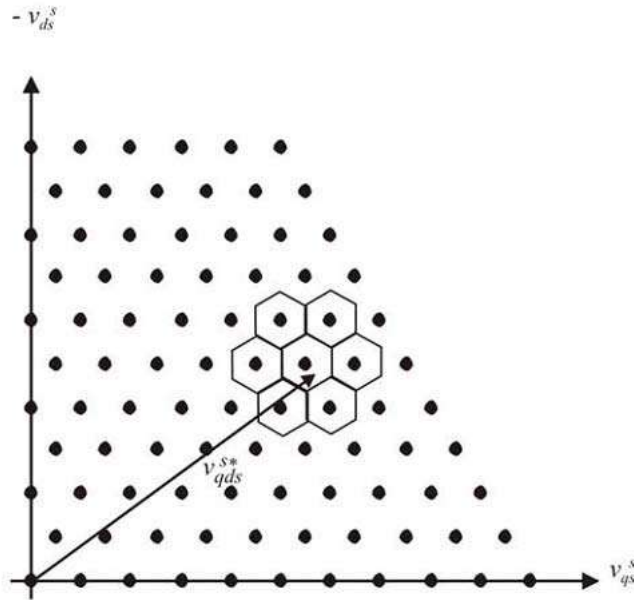**Figure.3.4. Duty cycle modulation voltage vectors.**

Figure 3.5. Eleven level space vector control

D. Space vector control

A rather unique voltage-source modulation method called space vector control (SVC) has been recently introduced. Since it is fundamentally different than sine-triangle or SVM, it is presented in this separate section. The premise of this scheme is that the inverter can be switched to the vector nearest the commanded voltage vector and held there until the next cycle of the DSP. Figure 3.5 illustrates the concept in the vector domain for an eleven-level inverter. Therein, only one quadrant of the vector plot is shown. The nearest vector to the commanded voltages is determined according to the hexagonal regions around each vector (some of which are shown in Figure 3.5). This operation is performed at each sample period of the DSP resulting in a simple modulation method. Since the vector is held for the DSP cycle, there is no need to compute switching times and schedule timing in the PLD.

Although this method is simple to implement, it is most useful on inverters with a relatively high number of voltage vectors. An example is the eleven-level series H bridge inverter with five cells. Another aspect of this control is that the DSP switching period should be small since the voltage is held constant for the entire switching time. Implementation of this scheme on an eleven-level inverter has shown that it can produce a lower THD than the SVM method.

3.2 Current-regulated methods

This section presents an overview of the current-regulated PWM schemes. An extension of the two-level hysteresis control is presented. Although this method directly regulates the currents, it relies on an analog implementation which is not practical for higher power levels. As a compromise, two new methods, referred to as clocked sigma-delta and multilevel delta modulation, are introduced. These schemes provide a digital implementation, but have lower harmonic performance than the voltage source methods.

The tradeoff between discrete implementation and harmonic performance has been an issue for current-regulated controls. For two-level power conversion, some researchers have proposed predictive control which relies on knowledge of the load parameters. Others have developed controls dependant on high-frequency timing of the current waveforms. These methods and others have been applied to multilevel power conversion.

A. Hysteresis control

The hysteresis current-control concept typically employed in two-level drive systems can be extended to multi-level systems by defining a number of hysteresis bands. This concept is illustrated in Figure 3.6 for the four-level inverter. The basic operation of the control involves defining n-1 evenly spaced hysteresis bands on each side of the commanded current. The voltage level is then increased by one each time the measured current departs from the commanded value and crosses a hysteresis band. One important detail of this control is that the voltage level will be at its highest or lowest value when the measured current crosses the lowermost or uppermost hysteresis band respectively. This ensures that the current will regulate about the commanded value. This straightforward extension of two-level current control results in good regulation of the currents and acceptable voltage level switching. Furthermore, the multi-level hysteresis control handles steps changes in commanded current with a response similar to two-level hysteresis control.

There are many other methods of implementing hysteresis band based current controls for multilevel inverters. The amount of analog circuitry can be reduced by using a single hysteresis band and increasing or decreasing the voltage levels each time the current touches the band. This method is then coupled with timing and a voltage controlled oscillator to drive the current error to zero. An extension to this method uses two hysteresis bands to provide better

dynamic performance, but still utilize a small amount of analog circuitry for a large number of voltage levels.

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B. *Clocked sigma-delta modulation*

Some current-regulated schemes are based on the sigma-delta function. As an example, the four-level sigma delta function is shown in Figure 3.7 for a phase. Based on the hysteresis level *h,* the per-phase switching state is determined from the current error. The function can be implemented directly with analog components or it can be implemented on a DSP based on a fixed clock frequency. In a two-level system, the hysteresis level is zero and the control reduces to that of standard delta modulation. As with two-level systems, the switching frequency of the inverter may be less than the clock frequency since the voltage level may not change every time the control is clocked. The current tracking improves with increasing clock frequency, and a relatively high frequency is needed for good performance. This makes the control somewhat undesirable, although digital implementation is an advantage.

The concept behind multilevel delta modulation is illustrated for the four-level system Figure 3.8. As with clocked sigma delta modulation, the control operates on a per-phase basis and can be implemented on a DSP. The general scheme functions by increasing or decreasing the voltage level by one at each clock cycle of the DSP depending on whether the current error is positive or negative respectively. In this control, the hysteresis band does not need to be defined. In the two-level implementation, the control reduces to that of standard delta modulation. As with clocked sigma-delta modulation, the clock frequency must be set relatively high in order to obtain good current tracking.
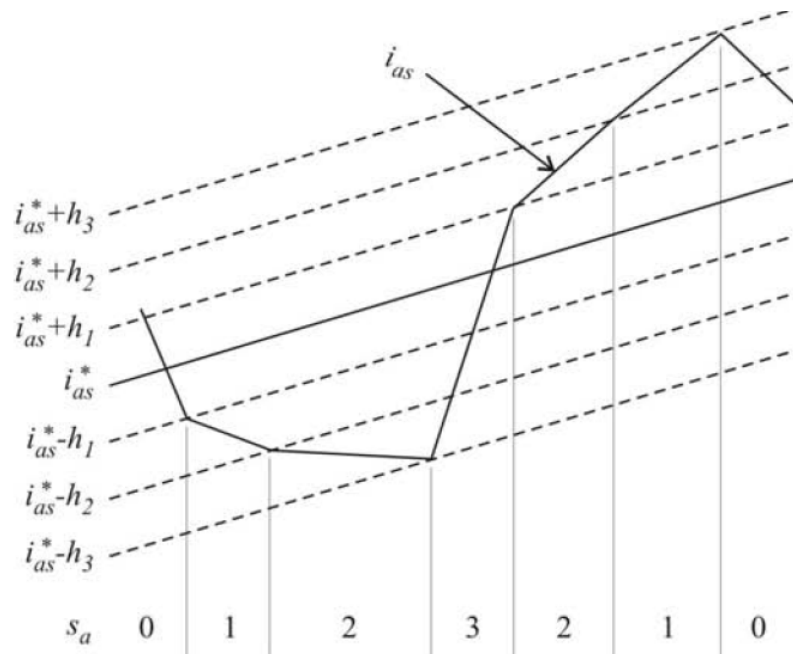
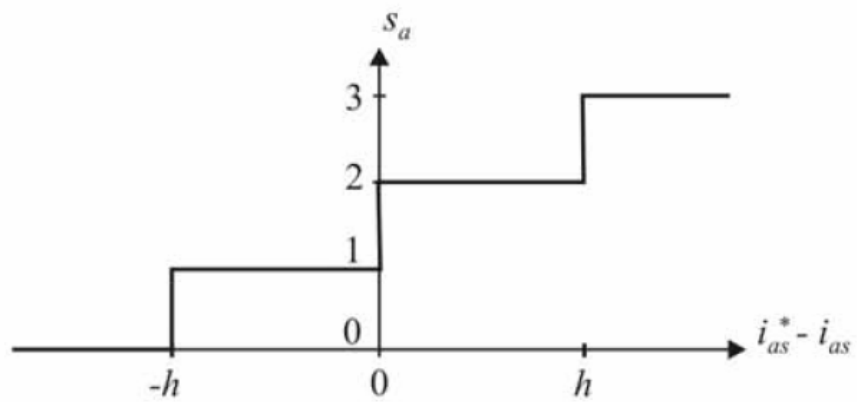**Figure 3.6 Ilustration of hystersis current control**
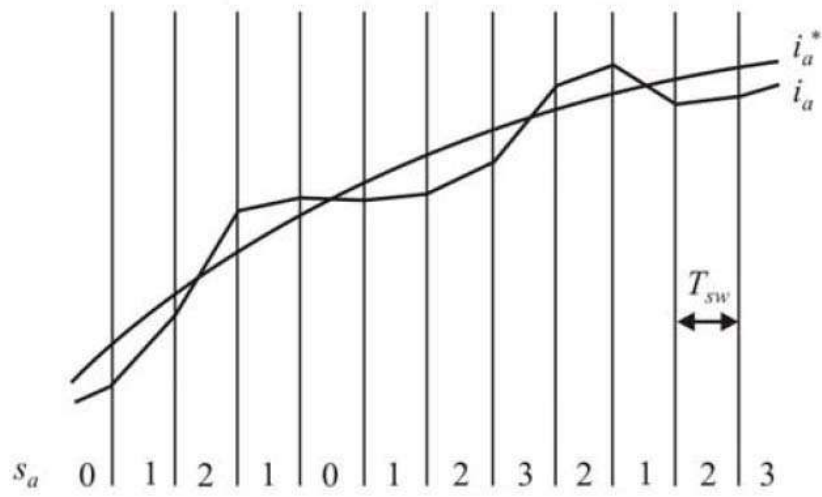

Figure 3.7 Fourlevel sigma delta function

Figure 3.8 Four level delta control scheme

Chapter 4

REDUNDANT STATE SELECTION

General Concept

4.1 General Concept

In previous chapters, it was noted that some inverter switching states are redundant in that there are several combinations that produce the same output voltages. Therefore, the exact inverter switching is not unique and this redundancy may be utilized to achieve certain goals. Among the possible redundant state selection (RSS) goals are

- ˌ Capacitor voltage balancing
- ˌ Reactor current sharing
- ˌ DC source current control
- ˌ Switching frequency reduction

It is also important to point out that two types of redundancy are possible. Joint phase RSS involves changing the common-mode voltage (that is increasing or decreasing the voltage level of all three phases). This was demonstrated in the first section during the discussion of voltage vectors. In the voltage vector plot, the joint phase RSS can clearly be seen by the voltage vectors achievable by more than one combination of switching states. For a particular set of switching states, the number of redundant states using joint-phase redundancy is given by (3.10). Per-phase redundancy refers to certain inverter topologies which have redundant switching states within each phase. An example of this is the flying capacitor topology where several transistor switching combinations lead to the same line-to-ground voltage.

The fundamental theory of RSS is to use inverter equations and operating conditions to determine the best redundant state to meet particular goals. In order to implement this concept, digital flags are created which represent inverter operation (capacitor voltage balance, current direction, etc.). The digital flags along with the modulator desired switching state form the input to an RSS table which can be filled off-line based on the inverter equations. Using this method, the best redundant state can be instantaneously selected during inverter operation.

Figure 4.1 shows a schematic of how the table can be included in a PLD. Based on the modified duty cycles, the DSP calculates the lower levels and switching times as described above. Many commercial DSPs have on-board PWM channels for two level operation. These may be loaded with the switching times and their two-level outputs ($PWMa$, $PWMb$, and $PWMc$) can be added to the lower levels in the PLD section to produce the switching states. Using this method, it is not necessary to have a modulation channel for each transistor pair. The switching states at this stage are commanded by the modulator and are denoted s_a*, s_b* , and

s_c^* .. In Figure 4.1, the digital flags include I_a, I_b, and I_c which indicate the direction of the a- b- and c-phase currents as well as flags indicating over- or under-charge for the inverter capacitors. Some analog circuitry will be required in order to generate the digital flags. More specifics on the digital flags will be given later. For now, it should be considered that the digital flags represent the state of the system relative to the RSS goals. This information is latched by the PWM modulator so that the information is only updated at the beginning of a PWM cycle. This prevents the table inputs from changing in the middle of a PWM cycle. The RSS table output is the final set of switching states that are sent to the inverter. At the top of Figure 4.1, an example of the possible output is shown. This example is identical to the previous example shown in Figure 3.4. Therein, the last PWM window has been changed by the RSS table from ($s_a^* = 2$, $s_b^* = 1$, $s_c^* = 0$) to ($s_a = 3, s_b = 2, s_c = 1$). As can be seen, the RSS switching can have an impact on the switching frequency. Typically, an increase in switching frequency is necessary in order to satisfy the RSS goals. The outputs of the RSS table are input to a breakout table which produces the transistor signals for a particular topology from the switching state as described above. In systems involving per-phase RSS, it is necessary to absorb this table into the RSS table making the table output the transistor signals.

Figure 4.2 shows the implementation of an RSS table in the DSP. In this case, the level and timing information for all phases is used to determine commanded switching states for the four windows labeled I, II, III, and IV. The DSP then performs four table look-ups based on the commanded switching states. For the digital flags, the analog signals (currents and capacitor voltages for example) are read into the DSP. After digital filtering, the flags are calculated. The result is a switching state for each window which includes the RSS. This information and the switching times are transmitted to the PLD through digital outputs where the PWM is implemented.
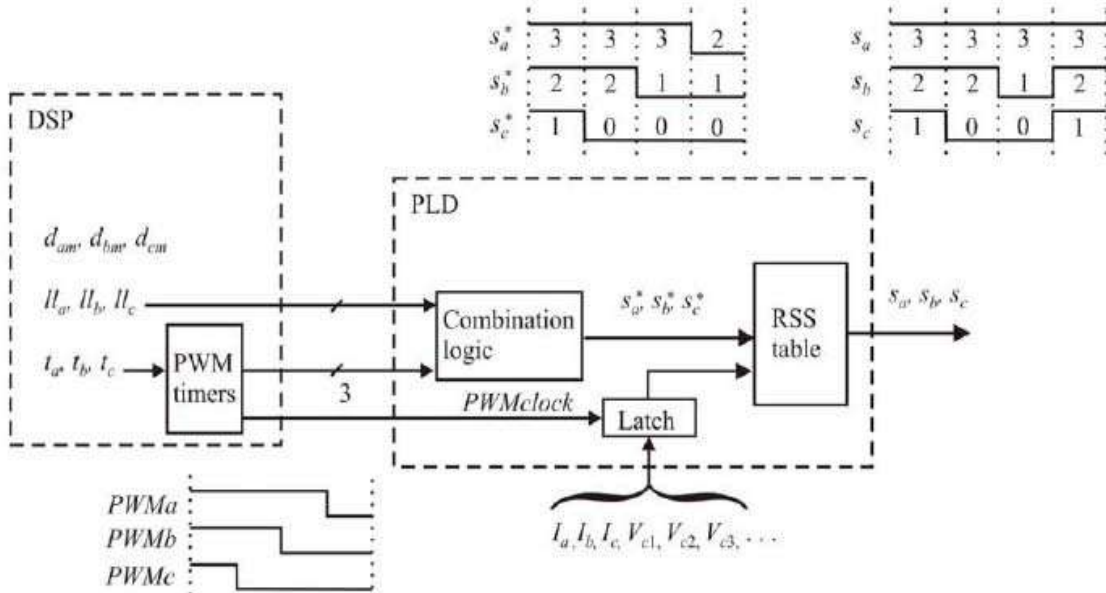
Figure 4.1 Redundant State Selection Implemented in PLD
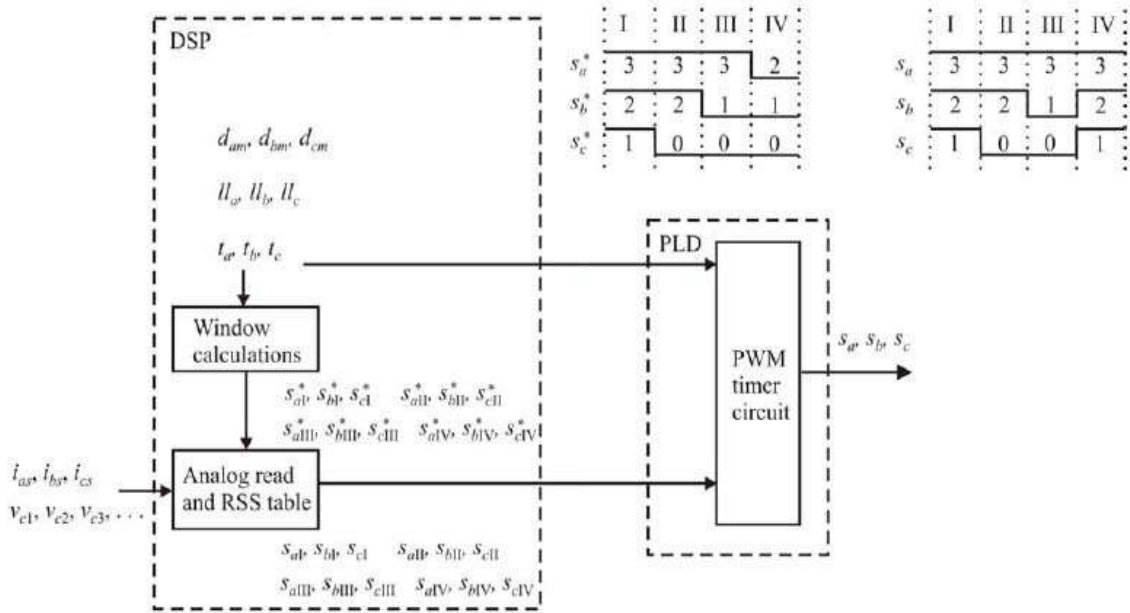
Figure 4.2 Redundant State Selection Implemented in DSP

chapter 5

RESULTS
Switching States

5.1 Diode Clamped Inverter
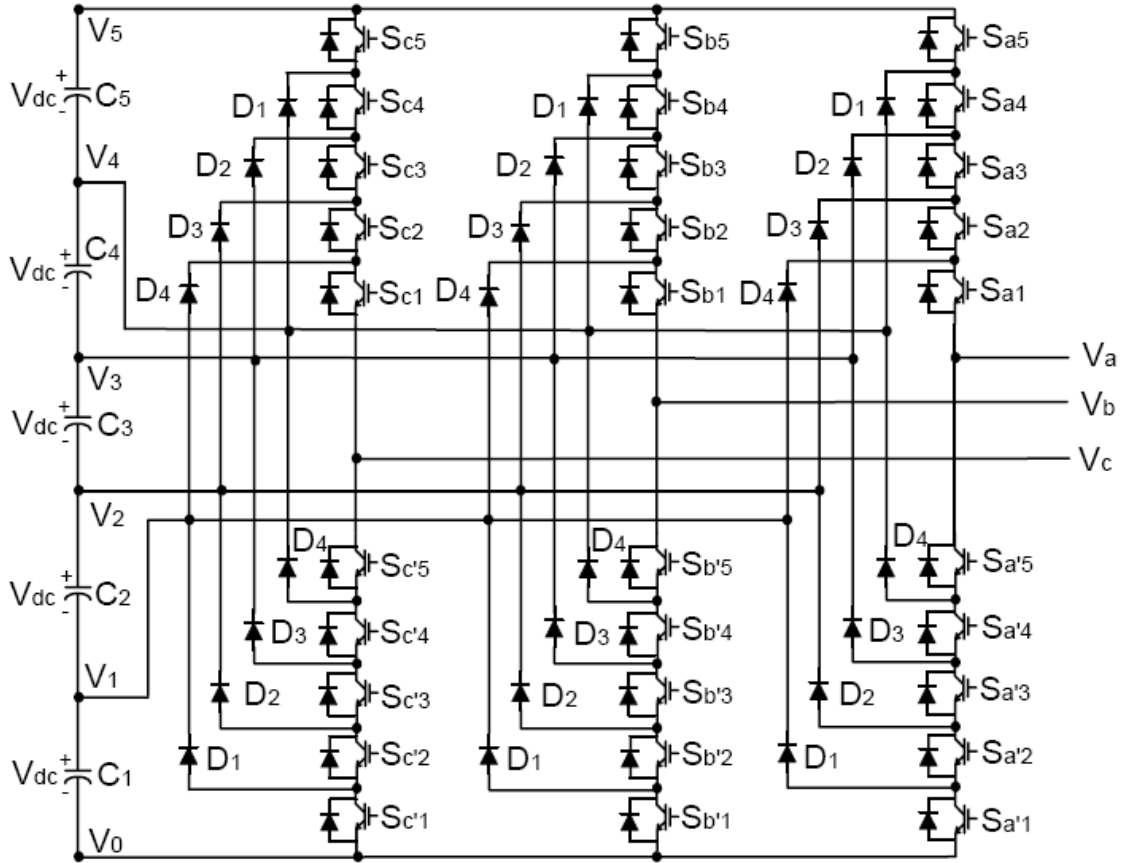
Figure 5.1 Three-phase six-level structure of a diode-clamped inverter

Table 5.1 diode clamped six level inverter voltage levels and corresponding switch states

Voltage V_{a0}	Switch State									
	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_5 = 5Vdc$	1	1	1	1	1	0	0	0	0	0
$V_4 = 4Vdc$	0	1	1	1	1	1	0	0	0	0
$V_3 = 3Vdc$	0	0	1	1	1	1	1	0	0	0
$V_2 = 2Vdc$	0	0	0	1	1	1	1	1	0	0
$V_1 = Vdc$	0	0	0	0	1	1	1	1	1	0
$V_0 = 0$	0	0	0	0	0	1	1	1	1	1

Figure 5.2 Line voltage waveform for a six-level diode-clamped inverter.

5.2 Flying Capacitor Inverter

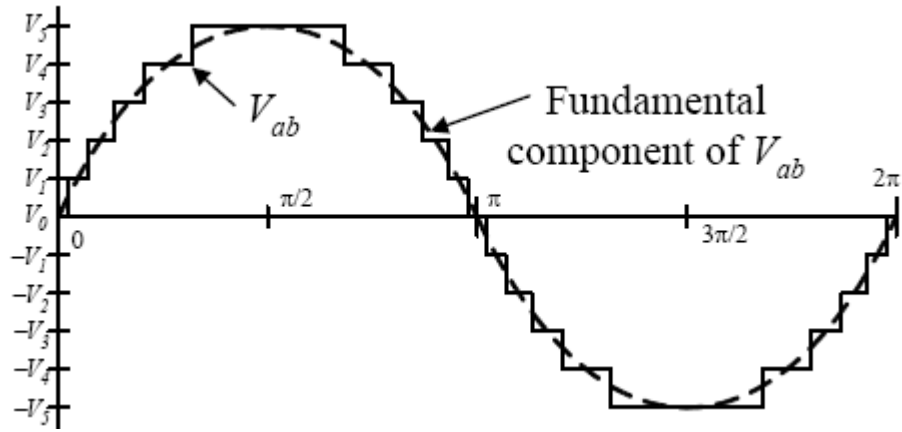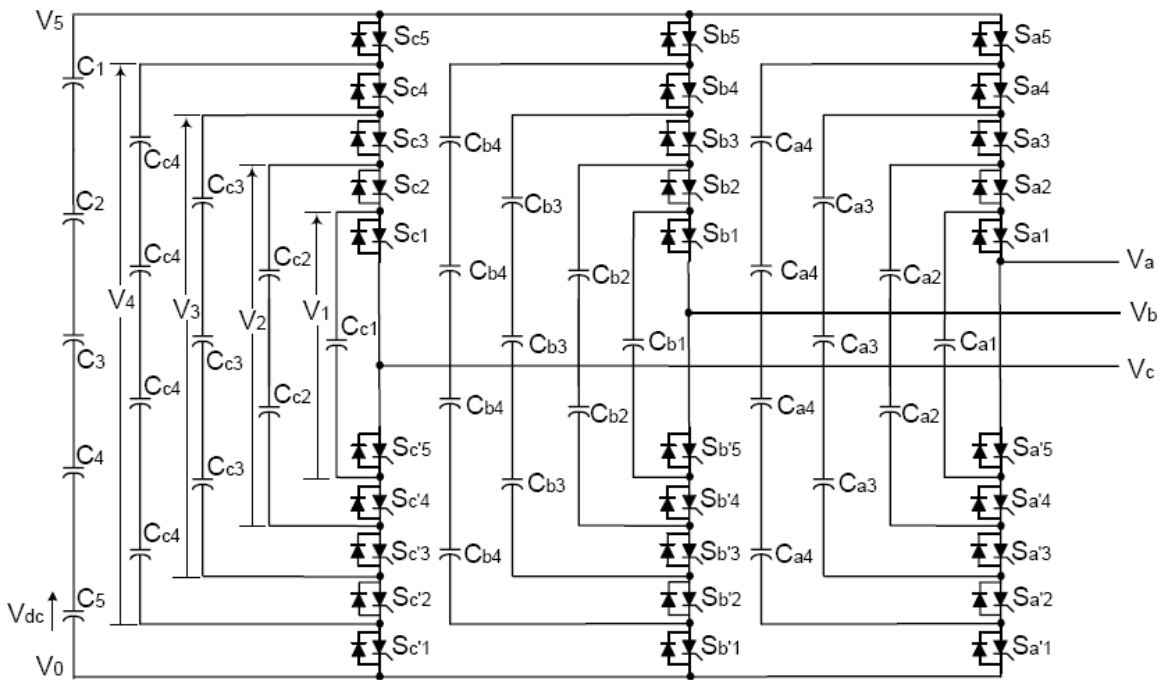**Figure 5.3 Three-phase six-level structure of a flying capacitor inverter**

Table 5.2 Flying-capacitor six-level inverter redundant voltage levels and corresponding switch states.

Voltage V_{a0}	Switch State									
	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_{a0} = 5V_{dc}$ (no redundancies)										
$5V_{dc}$	1	1	1	1	1	0	0	0	0	0
$V_{a0} = 4V_{dc}$ (4 redundancies)										
$5V_{dc} - V_{dc}$	1	1	1	1	0	0	0	0	0	1
$4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc}$	1	0	1	1	1	0	1	0	0	0
$5V_{dc} - 3V_{dc} + 2V_{dc}$	1	1	0	1	1	0	0	1	0	0
$5V_{dc} - 2V_{dc} + V_{dc}$	1	1	1	0	1	0	0	0	1	0
$V_{a0} = 3V_{dc}$ (5 redundancies)										
$5V_{dc} - 2V_{dc}$	1	1	1	0	0	0	0	0	1	1
$4V_{dc} - V_{dc}$	0	1	1	1	0	1	0	0	0	1
$3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc} - V_{dc}$	1	0	1	1	0	0	1	0	0	1
$5V_{dc} - 3V_{dc} + V_{dc}$	1	1	0	0	1	0	0	1	1	0
$4V_{dc} - 2V_{dc} + V_{dc}$	0	1	1	0	1	1	0	0	1	0
$V_{a0} = 2V_{dc}$ (6 redundancies)										
$5V_{dc} - 3V_{dc}$	1	1	0	0	0	0	0	1	1	1
$5V_{dc} - 4V_{dc} + V_{dc}$	1	0	0	0	1	0	1	1	1	0
$4V_{dc} - 2V_{dc}$	0	1	1	0	0	1	0	0	1	1
$4V_{dc} - 3V_{dc} + V_{dc}$	0	1	0	0	1	1	0	1	1	0
$3V_{dc} - V_{dc}$	0	0	1	1	0	1	1	0	0	1
$3V_{dc} - 2V_{dc} + V_{dc}$	0	0	1	0	1	1	1	0	1	0
$2V_{dc}$	0	0	0	1	1	1	1	1	0	0

$V_{a0} = V_{dc}$ (4 redundancies)										
$5V_{dc} - 4V_{dc}$	1	0	0	0	0	0	1	1	1	1
$4V_{dc} - 3V_{dc}$	0	1	0	0	0	1	0	1	1	1
$3V_{dc} - 2V_{dc}$	0	0	1	0	0	1	1	0	1	1
$2V_{dc} - V_{dc}$	0	0	0	1	0	1	1	1	0	1
V_{dc}	0	0	0	0	1	1	1	1	1	0
$V_{a0} = 0$ (no redundancies)										
0	0	0	0	0	0	1	1	1	1	1

chapter 6

CONCLUSION

Concluding Remarks

This thesis has demonstrated the state of the art of multilevel power converter technology. Fundamental multilevel converter structures and modulation paradigms including the pros and cons of each technique have been discussed. Most of the thesis focus has addressed modern and more practical industrial applications of multilevel converters. It should be noted that this thesis could not cover all multilevel power converter related applications; however the basic principles of different multilevel converters have been discussed methodically. The main objective of this thesis is to provide a general notion about the multilevel power converters and various modulation strategies mainly PWM techniques and their applications. We deduced possible switching states in six level diode clamped and flying capacitor Inverters

The general concept of multilevel power conversion was introduced more than twenty years ago. However, most of the development in this area has occurred over the past five years. Furthermore, each year seems to bring even more publications than the previous. Besides the mainstream power electronics conferences and journals, multilevel power conversion is also showing up in power systems and electronics societies. Despite the rapid growth of this area in recent years and the increasing number of innovations introduced each year, there is still much more that can be done.

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